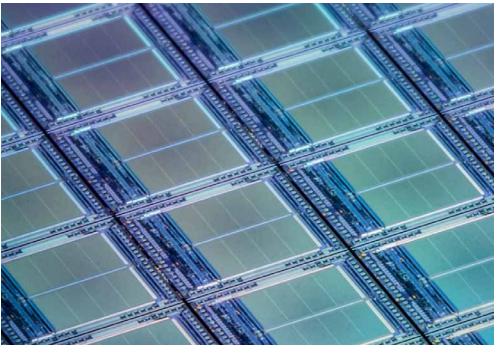


White Paper

iSLC – Claiming the Middle Ground of the High-end Industrial SSD Market



Summary

iSLC is a NAND flash technology designed to strike a balance between endurance, cost, and performance. This technology transforms MLC, TLC, and QLC NAND into SLC-like operation through firmware optimization, offering improved performance and a longer lifespan.

With the latest Ultra iSLC technology based on advanced 3D NAND architectures, the Program/Erase (P/E) cycles can reach up to 100,000 times.

In terms of the operating life test, iSLC outperforms 3D TLC devices under the same operating conditions. In write performance tests, iSLC demonstrates results comparable to SLC.

Introduction

Choosing the right storage solution involves balancing multiple factors—performance, capacity, and reliability. While high-density 3D NAND, such as TLC and QLC, provide competitive capacity, they can sometimes fall short in matching the endurance and performance requirements of critical applications. However, SLC delivers superior reliability but comes at a significantly higher cost, limiting its practicality.

iSLC technology was developed to offer a balanced solution that combines the endurance and reliability of SLC with the cost efficiency of mainstream NAND, addressing the trade-off. This white paper explains the differences among the NAND Flash technologies mentioned above and how iSLC has become a solution with broader applications for embedded and advanced product markets.

Background

With continuous advances in NAND manufacturing processes, manufacturers have developed methods to store multiple bits per cell, evolving from SLC (1 bit per cell) to MLC (2 bits), TLC (3 bits), and QLC (4 bits). These process innovations have enabled significant gains in storage density and cost efficiency, driving widespread adoption across the industry.

However, as more bits are stored in each cell, the number of voltage states also grows—8 for TLC, 16 for QLC, and up to 32 for PLC. At the same time, the voltage window between states becomes smaller, making cells more prone to interference and drift. This eventually affects the SSD's overall endurance, reliability, and lifespan.

Why does storing more bits per cell reduce fault tolerance?

SLC stores a single bit per cell, with only two voltage states separated by a wide margin. In contrast, for example, TLC with eight states divides the same voltage range into narrower intervals, resulting in easier state shifts of NAND cells from electrical noise or charge leakage compared to SLC NAND under the same conditions.

Although error correction codes (ECC) can recover many of these errors, the increase in raw bit errors still negatively affects performance. Therefore, lower error bit rates generally indicate better performance and reliability in NAND flash.

The increase in the bits that a cell can store causes the number of P/E cycles allowed per cell to decrease. Why?

There is an inherent problem in SSD: cell degradation. When a cell is programmed or erased, a relatively powerful electric field is generated, and this process slightly damages the cell substrate each time. The integrity of the substrate directly affects the cell's ability to maintain its state. The more P/E cycles there are, the more damage is done to the substrate, resulting in the cell having less ability to maintain its state.

SLC's wider voltage margin allows greater tolerance for substrate damage, and greater state drift is permitted without data misjudgment, making SLC more resilient to P/E cycle stress. In contrast, TLC is less tolerant of substrate damage from P/E cycles. The more P/E cycles a cell can endure, the longer the lifespan of the unit.

For general consumer use, 3D TLC and similar technologies remain beneficial due to affordability and sufficient durability. However, for industrial and enterprise applications, higher endurance and performance are often required, where 3D TLC may fall short.

SLC vs 3D TLC

While this section uses 3D TLC as a representative example of multi-layer NAND, the general principles also apply to other multi-bit NAND technologies such as QLC. The major difference between SLC and 3D TLC is the number of bits that each NAND cell holds. SLC stores 1 bit of data per cell, while 3D TLC stores 3 bits of data per NAND cell, which makes SLC more fault-tolerant than 3D TLC while supporting more P/E Cycles per cell. SLC offers improved durability and is an ideal choice for advanced applications. Other technical differences between SLC and 3D TLC include **programming time**, data retention, the P/E cycle, and the handling of error bits (as shown in Table 1).

	Program Page	Erase Block	P/E Cycle	Bits corrected by ECC
SLC (24nm)	400µs	4ms	60K	24 bit / 1024 Bytes
3D TLC	2300µs	10ms	3K	120 bit / 1024 Bytes

Besides faster speed, the raw bit error rate (RBER) of SLC, which is the number of written bit errors, is also lower. For example, if the sequence 01 01 01 01 is written as 01 11 11 01, two error bits have occurred. In the case of RBER, there are 2 error bits out of 8, resulting in an error rate of 0.25 or 25%.

The popularity of 3D TLC NAND is primarily driven by its low price, which enables NAND manufacturers to produce units of higher capacity at a more cost-effective rate compared to the more expensive SLC NAND. However, such a tradeoff will result in reduced reliability and durability, as shown in Figure 1. As NAND Flash technology has been upgraded from SLC to 3D TLC, manufacturers need higher ECC capabilities to compensate for the reduction in reliability and durability.

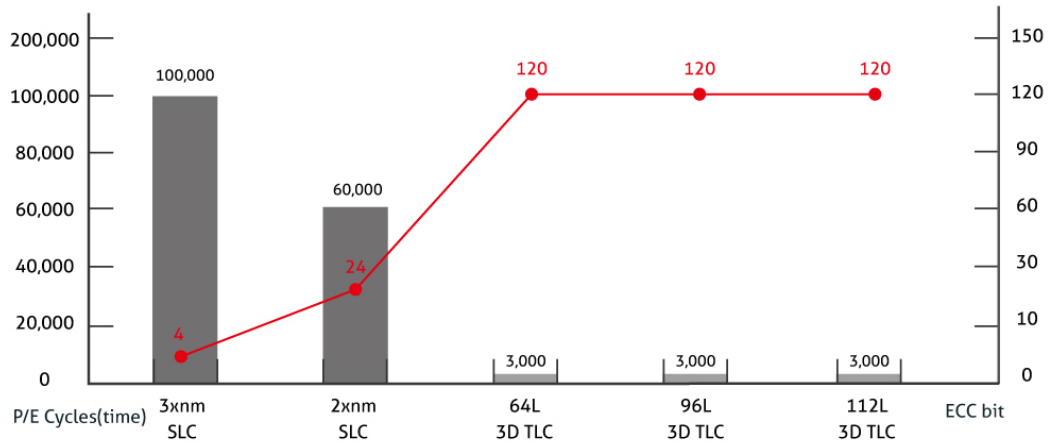


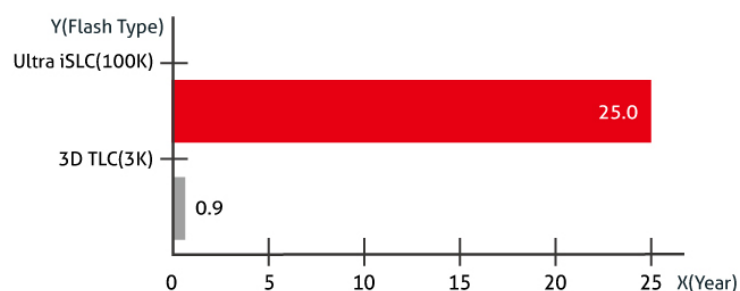
Figure 1 : NAND Flash Trend

Many applications fall between these two types of flash memory. 3D TLC is excluded due to performance and durability requirements. Therefore, system integrators have no choice but to use the more costly SLC options.

Cost-performance Optimization with iSLC

Ideally, iSLC should have a performance on par with SLC flash, while its cost is close to choosing a 3D TLC flash.

Figure 2 shows an example of increased durability. Using a 2TB SSD, with a Drive Writes Per Day (DWPD) rating of 10, the lifespan of an Ultra iSLC unit can still last for 25 years. In contrast, a 3D TLC unit can last about 1 year before failing. The lifespan of an Ultra iSLC unit is approximately 30 times longer than that of a 3D TLC unit.



Note: The above diagram is based on a test environment for a 100% sequential write.

Figure 2: Ultra iSLC and 3D TLC endurance comparison

iSLC allows 3D TLC flash to emulate the performance and durability of SLC cells through Innodisk's in-house designed firmware. iSLC can emulate SLC by having only 1 bit in each NAND cell (see Figure 3). Such firmware configuration enables the flash to function like SLC flash, which also enhances the durability and data retention levels of 3D TLC NAND flash.

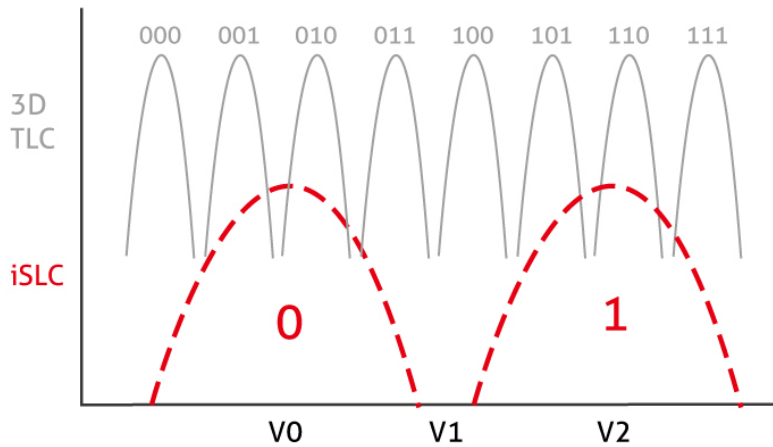


Figure 3: iSLC firmware technology

Test Data

The average durability of Ultra iSLC exceeds 100,000 P/E cycles, which significantly prolongs the service life of the drive when compared to a 3D TLC flash.

Our tests indicate that the error bits of Ultra iSLC are significantly lower than conventional multi-bit NAND, such as 3D TLC. When comparing the technology nodes of Ultra iSLC and conventional 3D NAND architectures (e.g., TLC), as the 112L Ultra iSLC P/E cycle reaches 100,000 times, the number of error bits is about 2. When the P/E cycle of 3D TLC goes 3,200 times, the number of error bits is about 16. Table 2 presents a comparison of the number of error bits between Ultra iSLC and 3D TLC.

Table 2: Error bits Comparison between Ultra iSLC and 3D TLC		
Flash Type	Average Erase Count	Error bit
Ultra iSLC	100,000	2 bits / 1024 Bytes
3D TLC	3,200	16 bits / 1024 Bytes

Note.

1. The number of error bits that 3D TLC series controllers can fix all reaches 120bits/1KB, which means that when the PE cycle reaches the guaranteed number of times, the occurrence of error bits is still substantially within the range of the controller's fixing ability
2. The above values are for reference only. The occurrence of the error bit will vary according to the actual usage
3. Innodisk introduced Ultra iSLC technology, a breakthrough that allows the endurance of 3D TLC to reach **100K P/E cycles**. This advancement further expands iSLC's applicability, providing an even more durable solution for critical industrial uses while retaining the cost advantages of 3D TLC.

Conclusion

- The advantages of iSLC and Ultra iSLC can be summarized as:
- Extended lifetime and improved reliability compared to 3D TLC
 - Performance similar to SLC
 - More cost-efficient than SLC
 - Data retention and a five-year warranty

Ultra iSLC bridges the gap between the cost-effectiveness of multi-bit NAND and the endurance and performance of SLC. These attributes make Ultra iSLC an ideal storage solution, particularly well-suited for the high-end industrial and embedded products markets, where cost-efficiency is in demand and product durability is non-negotiable.

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The logo for Innodisk Corporation, featuring the word "innodisk" in white lowercase letters on a red rectangular background. A small red square is positioned at the top right corner of the main red rectangle.

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